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Configurable Joint Detection Algorithm for MIMO Wireless Communication System

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Abstract - VLSI architecture of a configurable joint detection and decoding (CJDD) scheme for multi-input multi-output (MIMO) wireless communication systems with convolutional codes. A novel tree-enumeration strategy is proposed such that the MIMO detection and decoding of convolutional codes can be conducted in single stage using a tree-searching engine. Moreover, this design can be configured to support different combinations of quadrature amplitude modulation (QAM) schemes as well as encoder code rates, and thus can be more practically deployed to real-world MIMO wireless system. A formal outline of the proposed algorithm will be given and simulation results for 16-QAM and 64-QAM with rate-1/2 andrate-1/3 codes will be presented showing that, compared with the conventional separate scheme, the CJDD algorithm can greatly improve bit error rate (BER) performance with different system settings. In addition, the VLSI architecture and implementation of the CJDD approach will be illustrated. The architectures and circuits are designed to support configurability and flexibility while maintaining high efficiency and low complexity. The post layout experimental results for 16-QAM and 64-QAM withrate-1/2 and rate-1/3 codes show that, compared with the previous configurable design, this architecture can achieve reduced or comparable complexity with improved BER performance.

Keywords: Circuit, Convolution codes, joint detection and decoding (JDD), multi-input multi output (MIMO) detection, Bit Error Rate.

I.INTRODUCTION

MIMO technology improves performance of wireless links, at the cost of high computational complexity both at transmitter and receiver sides. In particular, at the receiver end, the detector has to recover from the received signal vector the original data stream corresponding to each transmitting antenna Coded MIMO systems is the Maximum Likelihood detector (ML) [1]-[2]. the List Sphere Decoder (LSD) was first introduced into enable joint detection and decoding; single tree search is exploited in as an alternative to repeated tree search technique to improve computational efficiency; a smart management of the tree search is proposed into achieve low complexity. However, fully exploiting these gains comes, in general, at the cost of significantly increased signal-processing complexity, especially in the receiver.

The physical layer of a receiver for MIMO wireless systems consists of several parts, such as radio frequency (RF) components, synchronization circuitry, channel estimation, and the MIMO decoder [3]-[4]. The MIMO decoder consists of a MIMO detector to separate the spatially multiplexed data streams and a channel decoder, which computes estimates of the transmitted information bits.

II.EXISTING SYSTEM

a) System Analysis

The existing algorithm and VLSI architecture of a configurable JDD (CJDD) scheme that can conduct the MIMO detection and decoding of convolutional codes currently [5]. More importantly, the proposed design is greatly improved such that it can be configured to operate with different combinations of encoder code rates and QAM modulation schemes, the most commonly used modulation schemes in contemporary wireless systems. This is achieved through the proposal of a novel tree-searching strategy where its enumeration scheme can be adjusted according to the employed system parameters. Compared with the previous JDD method depicted in this architecture can be applied to a more generalized domain

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of MIMO communications and can be practically deployed to real-world wireless systems. In other words, the conventional channel decoder component, such as the Viterbi decoder is no longer needed [6].

The algorithm and VLSI architecture of JDD scheme depicted in compared with the conventional separate structure, a 2–2.5 DB improvement of BER can be achieved with comparable system complexity without any iteration [7]. However, the JDD method has a prominent weakness that, due to the limitation of the utilized tree-enumeration scheme, it can only operate in the system with dedicated configuration, that is,16-quadrature amplitude modulation (QAM) with rate-1/2convolutional codes [8]-[9].

III.PROPOSED SYSTEM

a) Joint Detection and Decoding

A high-level architectural (CJDD) processor is proposed. BPSK modulation scheme is used. A simple case of the mapping performed by the encoder is the uncoded transmission, where the symbols in the codeword are independent of each other. Consider the AWGN channel with uncoded transmission, where the encoder transmits one of two symbols, −1 and +1, with equal probability during each channel use. Note that x(t) is the output of the encoder corresponding to the message intended for transmission by the source, out of 2Nequally likely messages [10]. Given the output sequence y ∈ RN at the destination, the task of the detector is to determine the sequence transmitted by the source. it can only operate in the system with dedicated configuration, that is,16-quadrature amplitude modulation (QAM) with rate-1/2convolutional codes.

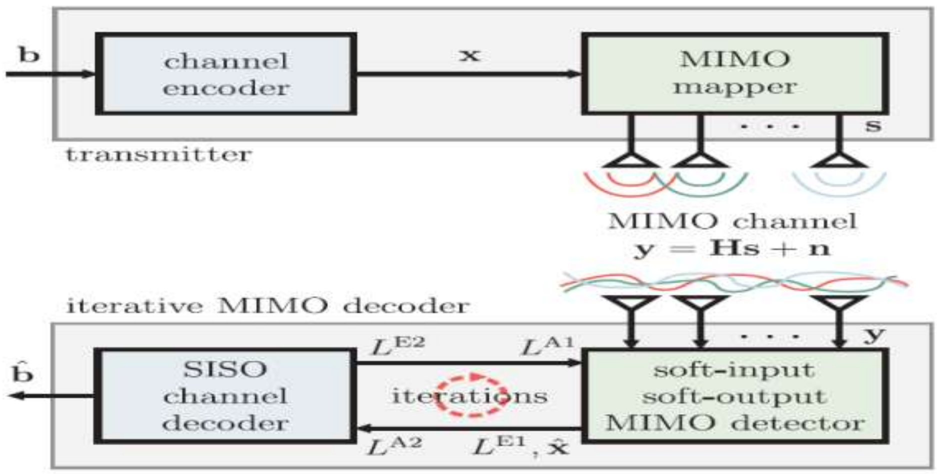

Figure-1: MIMO wireless communication system employing BICM, spatial multiplexing (SM), and iterative MIMO decoding

b) Tree search algorithms

Recent years have witnessed a growing interest in the closest lattice point search (CLPS) problem. This interest was increased by the connection between CLPS and maximum likelihood (ML) detection in multiple-input multiple-output (MIMO) channels. MIMO channels offer significant advantages in terms of increased throughput and reliability at the price of a more challenging decoding task for the receiver. For example, the exhaustive search implementation of ML detection has a complexity that grows exponentially with the degrees of freedom, m, available in the channel.

c) *Soft-Input Soft-Output MIMO Detection*

Iterative MIMO decoding requires soft-input soft-output (SISO) detection schemes to compute a posteriori reliability information for the coded bits based on the received vector, on channel state information, and on a priori reliability information. In order to perform this task, a variety of algorithms exists in the literature. The optimum SISO detection method and a prominent low-

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complexity algorithm are described below. In the remainder of this section, we only focus on the MIMO detector and omit the superscript 1 in the LLR notation, i.e., we write LA and LE instead of LA1 and LE1, respectively.

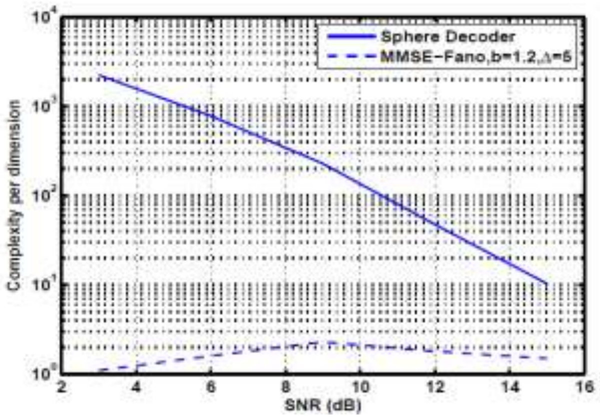

Figure.2: Complexity of the SE sphere decoder and the MMSE-DFE Fano decoder with TAST constellations, for the 4 × 4 MIMO channel

d) MIMO technology

The overriding goal of our work is to establish a general framework for the design and analysis of tree search algorithms for joint detection and decoding. Towards this goal, we first divide the decoding task into two interrelated stages; namely (1) preprocessing and 2) tree search. The preprocessing stage is primarily concerned with exposing the underlying tree structure from the noisy received signal.

The MMSE-DFE Fano decoder emerges special here; we discuss the integral roles of minimum mean square error decision feedback equalizer (MMSE-DFE) filter, lattice reduction techniques, case of our general framework that enjoys a favorable performance-complexity tradeoff. We establish the superiority of the proposed decoder via numerical results and analytical arguments in several relevant scenarios corresponding to coded as well as uncoded transmission over MIMO and inter-symbol-interference (ISI) channels. More specifically, in our simulation experiments, we apply the tree search decoding framework to uncoded BLAST, linear dispersion space-time codes, algebraic.

e) Taming the Channel: Left Preprocessing

In the case of uncoded transmission (G = I), QR decomposition of the channel matrix H (assuming rank(H) = m) allows one to employ a simple recursive detection algorithm of the information symbols x. Indeed, Q is the feed forward matrix of the zero-forcing decision feedback equalizer (ZF-DFE).

f) Generic Branch and Bound Algorithm

Before describing the proposed algorithm, we first need to introduce some more notations. ACTIVE is an ordered list of nodes. The search algorithm to terminate when the numbers of nodes generate increases beyond a tolerable limit on the complexity. Whenever a leaf node reaches the top of ACTIVE, ˆx is updated if appropriate. Now, we use GBB to classify various tree search algorithms in three broad categories. This classification highlights the structural properties and advantages/disadvantages of the different search algorithms.

g) Inducing Sparsity: Right Preprocessing

In order to obtain the tree structure, one needs to put R1G in upper triangular form R (e.g., via QR decomposition). The sparser the matrix R, the smaller the complexity of the tree search algorithm. For example, a diagonal R means that symbol-by-symbol detection is optimal, i.e., the tree search reduces to exploring a single path in the tree. Loosely, if one adopts a depth first search strategy, then a sparse R will lead to a better quality of the first leaf node found by the algorithm consequently, the algorithm finds the closest point in a shorter time. Lattice reduction finds a reduced lattice basis, i.e., the columns of the reduced generator matrix S has small norms and are as orthogonal as possible.

The most widely used reduction algorithm is due to Lenstra, Lenstra and Lov´asz (LLL) and has a polynomial complexity in the lattice dimension. An enhanced version of the LLL algorithm, namely, the deep insertion modification, was later proposed by Schnorr and Euchner.

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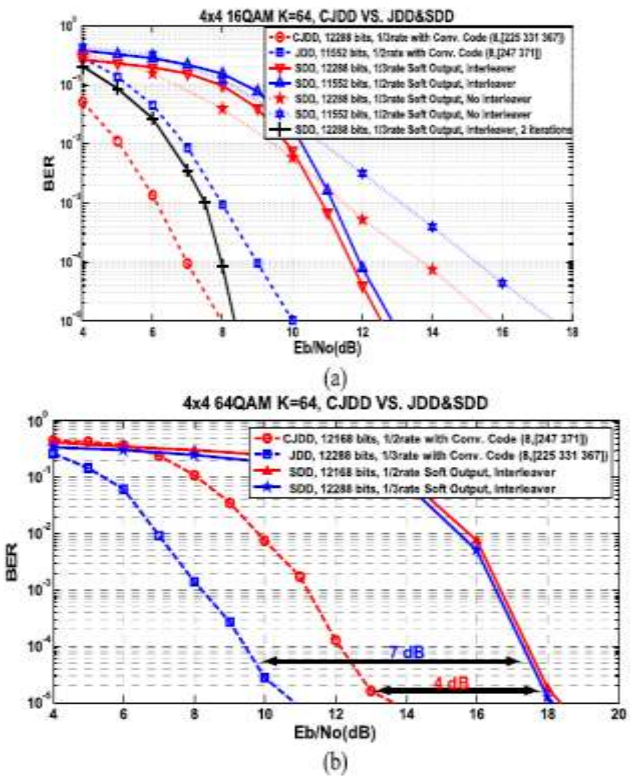

Figure.3: BER performance comparisons between CJDD, JDD, and conventional SDD (a) 16-QAM and (b) 64-QAM modulation scheme

LLL with deep insertion gives reduced basis with significantly shorter vectors. In practice, the complexity of the LLL with deep insertion is similar to the original LLL even though it is an exponential time algorithm in the worst case.

IV.SOFTWARE SPECIFICATION

Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

1. Modelsim

2. Xilinx

User Interface

The primary user interface of the ISE is the Project Navigator, which includes the design hierarchy (Sources), a source code editor (Workplace), an output console (Transcript), and a processes tree (Processes). The Design hierarchy consists of design files (modules), whose dependencies are interpreted by the ISE and displayed as a tree structure. For single-chip designs there may be one main module, with other modules included by the main module, similar sub routine in C++ programs. Constraints are specified in modules, which include pin configuration and mapping. The Transcript window provides status of currently running operations, and informs engineers on design issues. Such issues may be filtered to show Warnings, Errors, or both.

V.SIMULATION

System-level testing may be performed with ISIM or the ModelSim logic simulator, and such test programs must also be written in HDL languages. Test bench programs may include simulated input signal waveforms, or monitors which observe and verify the outputs of the device under test. ModelSim or ISIM may be used to perform the following types of simulations: Logical verification, to ensure the module produces expected results. Behavioral verification, to verify logical and timing issues. Post-place & route simulation, to verify behavior after placement of the module within the reconfigurable logic of the FPGA.

VI.RESULT

This research thesis deals with the theme of MIMO detection, both hard and soft. It focuses on algorithmic, architectural and implementation aspects of the Sphere Decoder Algorithm and one of its soft versions, the List Sphere Decoder. From a detailed analysis on the state of the art, software models and architectural issues, some critical aspects become relevant: the throughput and the flexibility. A formal outline of algorithm is given and simulation results are presented showing that the proposed CJDD algorithm can greatly improve the BER performance with different system settings.

VII.CONCLUSION

In comparisons between the CJDD and the conventional the implementation of an iterative receiver presented in also elucidates design tradeoffs and provides

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valuable insights. In particular, this paper reported a FPGA-based iterative receiver design based on the QPSK modulation and Minimum Mean Square Error MIMO detector. Required logic elements increase by ~70% and the memory requirement increases ~5×.improve performance with multiple iterations between the detector and the decoder, with the cost of significantly increased hardware complexity and degraded throughput.

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