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Investigating Electro-Thermal Coupling in Three-Dimensional Integrated Systems: Simulation Design Advances and Mitigation Strategies

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***Abstract* - Three-dimensional integrated systems employing vertical stacking technology and through-silicon via (TSV) interconnects offer enhanced performance and reduced power consumption. However, TSV technology introduces elector-thermal coupling phenomena, compromising the reliability and efficiency of these systems. This study provides a comprehensive review of simulation design advancements for elector-thermal coupling in TSV-based three-dimensional integrated circuits. Electrical and thermal simulation methodologies are elucidated and potential impacts and mitigation strategies are thoroughly explored. A systematic analysis is presented to elucidate the challenges and optimization opportunities in elector-thermal coupling, informing future research directions.**

Keywords: Three dimensional integrated circuits, (3D-ics); through silicon via tsv technology; Electro thermal coupling; simulation design; thermal electric modeling.

I. INTRODUCTION

With the further reduction of feature size and the advancement of integration scale, with the continuous expansion of transistors, the physical size of transistors has approached the limit of device technology. The strategy of improving performance only by reducing the feature size has become increasingly restricted, and Moore's Law is facing severe challenges. Three-dimensional integrated circuits (3D-ICs) greatly reduce the number of interconnects by enabling vertical stacking of devices. Length, thus reducing signal transmission delay and promoting the solution of interconnects delay-related problems. This approach not only shortens the gate delay, but also reduces load capacitance and resistance by using shorter traces. Stacking memories such as dynamic random-access memory (DRAM) above the processor core can significantly increase the bandwidth between the processor and the memory, while vertical stacking between different processor cores can increase the bandwidth of inter-core communication. The basis of these methods lies in efficient vertical interconnects technology, represented by through silicon vias (TSV), which are an integral part of vertical stacking. TSV and other forms of vertical interconnection methods reduce the length of the internal interconnection lines of the chip, effectively increase the signal transmission rate, reduce the interconnection delay, improve the integration level and operation speed of the circuit, and at the same time bring more Low power consumption and better performance. However, this technological innovation also brings unprecedented challenges to the thermal management and reliability of electronic devices. Multi-chip integration in 2.5D and 3D packaging not only increases the number of transistors and heat generation, but also results in higher heat density due to packaging area limitations. Chips located at the bottom and middle of the stack face greater heat dissipation problems because the stacked package is not easy to dissipate heat. The TSV is surrounded by closed structures such as insulation layers, chips, and substrates, which further increases the difficulty of heat dissipation. The combined effect of these factors may cause the chip temperature to rise sharply, [1, 2] endangering the reliability and long-term stability of the device. At the same time, the increase in chip temperature will in turn affect the temperature of the conductor, resulting in changes in its electrical conductivity, thermal conductivity, thermal expansion coefficient and other parameters, thereby causing the gap between the electric field and the thermal field. Forming a mutually coupled iterative relationship affects the transmission and distribution of current. Only when the chip reaches thermal equilibrium and the distribution of current and heat is stable, the Electrothermal coupling effect will terminate. The Electrothermal effects of interconnect solder joints and transmission lines are affected and taken into account. In order to deal with these thermal issues and ensure the reliability of 3D-IC, comprehensive Research shows that when considering electrothermal coupling effects, a sophisticated model must be established to simulate and analyzed the distribution and interaction of heat and current in a chip [3]. FAKHREDDINE et al. [4] performed signal and thermal analysis of a three-dimensional stacked resistive

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switch random access memory array. ZHOU et al. [5] developed a finite element simulation model for multi-layer chip stacking and analyzed the electrothermal effect of the entire chip under current load, including the temperature and electric field distribution, as well as the thermal stress distribution at the solder joints. BELKHIRIA et al. [6] examined the self-heating effect of transistors in the chip. CHAI et al [7, 8] analyzed the electrothermal effect of array TSVs, considered the effect of a Gaussian pulse voltage load, and proposed the radial point interpolation method to study the transient electrothermal effect of TSVs. They also analyzed the influence of TSV structural parameters on the electrothermal coupling effect. Thermal management measures are crucial to ensure that thermal issues are considered at both the design and operational levels, maintaining the system's normal operation within a safe temperature range. To achieve this, it is essential to develop efficient heat dissipation technology, design structures with improved thermal conductivity, and adopt thermal management strategies such as dynamic thermal management technology and thermal interface materials. Research by Zhang et al. [9] has explored the heat transfer principles of three-dimensional stacking systems and evaluated the thermal performance of various thermal management strategies, including natural convection, direct cooling, micro-channel cooling, and top heat dissipation. Their study clarifies the principles and effects of each method, highlighting their applicable conditions and potential limitations. While natural convection is effective for systems with lower power consumption, it may be insufficient for high-power devices. In contrast, direct cooling and micro-channel cooling offer better heat dissipation but increase system complexity and cost. Top heat dissipation provides an effective solution for vertical heat transfer in three-dimensional stacking systems. Researchers have explored various micro-channel heat dissipation structures to enhance thermal management in electronic devices. ZHU et al. [10] used numerical simulation to investigate the heat transfer performance of micro-channels with water droplet cavities and fins, finding that elliptical fins and cavity structures offer the best thermal performance. ALFELLAG et al. [11] studied the impact of pin fin diameter ratio and fin number on heat transfer efficiency in micro-channels. DING et al. [12, 13] developed a simulation model for a processor with a micro-channel fin heat dissipation structure, analyzing temperature distribution and channel flow characteristics to optimize design and reduce core temperature. FENG et al. [14, 15] proposed an embedded gradient distributed micro fin array microchannel, demonstrating its heat transfer advantages through numerical simulation and experimentation. KAUL et al. [16] designed an embedded micro-channel heat dissipation structure for FPGA, achieving a core temperature of 30°C and thermal resistance of 0.074°C/W at 107W chip power consumption. XU et al. [17] established a fast thermal analysis model for 3D layout planning and proposed a TSV allocation scheme to minimize chip temperature.

1.1 TSV Electrical Simulation in 3D ICs

As chip technology advances, accurate electrical characteristics of Through-Silicon Vias (TSVs) become increasingly crucial, directly impacting system performance and reliability. To extract TSV parasitic parameters, researchers have conducted extensive studies on lumped parameter models and numerical calculation models. The TSV lumped parameter model focuses on electrical characteristics, involving parameter extraction such as equivalent resistance, capacitance, and inductance, which represent TSV's actual circuit behavior. This model provides designers with a quick evaluation of TSV electrical performance during initial design or at lower frequencies. Numerical calculation models, employing complex methods like Finite Element Analysis (FEA), are used to simulate current, voltage, and electric field distribution in detail, offering a more accurate analysis of TSV characteristics. These models are essential for a comprehensive understanding of TSV behavior, enabling designers to optimize system performance and reliability.

1.2 Electrical simulation design based on lumped parameter model

The research explores the development of a TSV lumped parameter model, incorporating the effects of TSV diameter, height, insulation layer thickness, material composition, grounding spacing, and signal propagation velocity. Hu et al. [18] developed an equivalent RLGC circuit model for cylindrical TSVs, presenting analytical expressions for resistance, inductance, conductance, and capacitance parameters (Figure 1). Their work also encompassed frequency-domain and time-domain analyses to investigate TSV signal integrity, impedance, and electrical performance. Recent studies have advanced the modelling of Through-Silicon Vias (TSVs) for 3D integrated circuits (3D-ICs). Fu et al. [19] developed an accurate electrical model for cylindrical TSVs, incorporating the capacitance effect of metal-oxide-semiconductor (MOS) structures. Xu et al. [20] presented a comprehensive and accurate compact RLGC model, applicable to 3D-IC TSVs across low- to high-frequency ranges. Their model accounts for MOS effects, AC conduction, skin effects, and eddy currents in silicon substrates, including carbon nanotube (CNT) bundle TSVs. Notably, they introduced coaxial TSVs, leveraging the outer metal layer's shielding effect to minimize signal crosstalk. Building on this concept, Lu et al. [21] proposed a coaxial ring TSV broadband equivalent circuit model. Using Bessel

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functions, they derived closed-form expressions for resistance and inductance. Validation through a 3D high-frequency electromagnetic field solver (HFSS) yielded maximum errors of 6.5% (R), 1.7% (L), 5.5% (G), and 1.8% (C). Salah et al. [22] Salah et al. [22] presented a compact lumped model for Through-Silicon Vias (TSVs), accounting for physical dimensions and material properties (Figure 2). Their model provides closed-form expressions for capacitance, resistance, and inductance coupling. Electromagnetic simulations validated the model's accuracy, revealing a maximum discrepancy of less than 6% between predicted and simulated results. Recent studies have advanced the modeling and analysis of Through-Silicon Vias (TSVs) for 3D integrated circuits (3D-ICs). Lu et al. [23] proposed an equivalent circuit model for Shielded Differential TSVs (SDTSVs) (Figure 3) and validated it using 3D HFSS, demonstrating high accuracy up to 100 GHz. They also introduced a full-wave extraction method for RLGC parameters applicable to differential transmission lines. Savidis et al. [24] developed a data-fitting-based calculation equation for TSV RLGC models, achieving maximum errors of less than 8% for R, L, and C. Rao [25] investigated tapered TSVs' electrical properties, comparing Cu/CNT-filled tapered and cylindrical vias. Results showed a return loss below 20 dB at 30 GHz, suitable for high-frequency applications. Hu et al. [26] designed a compact Differential Multi-Bit CNT TSV (DMC-TSV) using multi-bit TSVs (Figure 4). Weerasekera et al. [27] established an RLC model based on data fitting, though omitting oxide and depletion layer thickness considerations. Simulation results revealed a maximum error of less than 6% between model predictions and actual results. Katti et al. [28] developed an analytical model for depletion layer capacitance in Through-Silicon Vias (TSVs), correlating capacitance with depletion region width. Numerical simulation verification yielded a high degree of accuracy, with maximum errors below 3.52%. Kim et al. [29] proposed and verified a scalable TSV electronic model in high-frequency scenarios and analyzed the electrical behavior of the model under different design parameters.

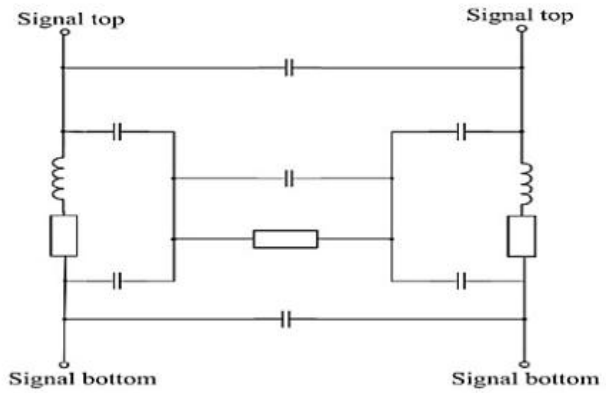

Figure 1: Equivalent RLGC model of cylindrical TSV

1.3 Electrical simulation design based on lumped parameter model

When performing numerical model calculations on three-dimensional integrated circuits, the three commonly used analysis models are the finite difference method (FDM) model, the finite element method (FEM) model, and the finite volume method (FVM) model. The FDM model theory is mature and has a rich practical basis. It can adapt to various accuracy requirements, has excellent parallelism, can handle complex areas, and is more suitable for modelling complex physical models. However, this method encounters difficulties when dealing with irregular areas, such as the complexity of boundary processing.

This property may lead to larger numerical dispersion and error accumulation, as well as higher computational costs. Based on FDM, DAHL et al. [30] developed a novel vertically interconnected local field modeling approach for cylindrical Through-Silicon Vias (TSVs) using rectangular grids. This method leverages the FDM framework to derive sparse matrices via the discretization of Maxwell's equations, enabling accurate computation of TSV impedance characteristics. Recently, significant advancements have been made in modeling Through-Silicon Vias (TSVs) for three-dimensional integrated systems. HUANG et al. [31] developed a Metal-Oxide-Semiconductor (MOS) capacitance model for TSVs using the Finite Difference Method (FDM), enabling efficient calculation of insulating and depletion layer point distributions with a single iteration. Building on this progress, XIE et al. [32] introduced an efficient methodology for modeling TSV signal paths in silicon interposers. Their established model accurately predicts parasitic effects in multiple transmission lines. Figure 5 illustrates the five RDL-Transition structures and cross-sectional views of TSV-RDL, providing valuable insights into the intricate relationships between TSV and redistribution layer (RDL) designs.

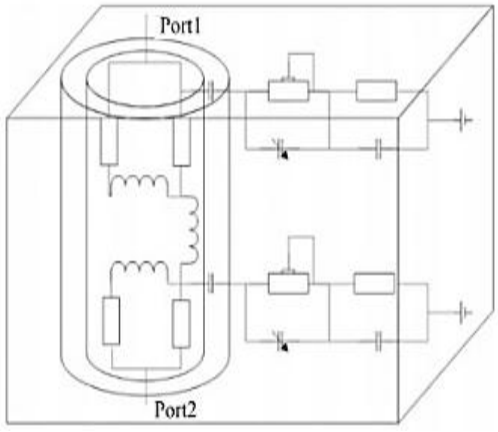

Figure 2: TSV lumped model based on a single structure

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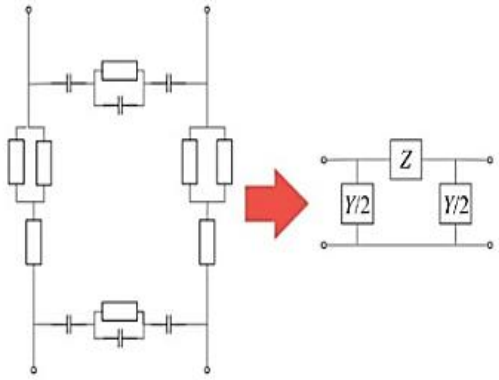

Figure 3: Equivalent circuit model of shielded

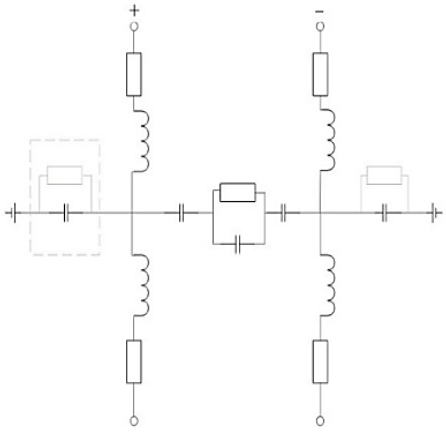

Figure 4: Compact DMC-TSV

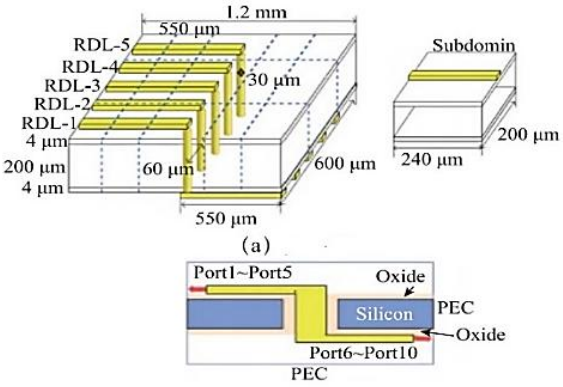

Figure 5: cross sectional view

The application of FEM in three-dimensional integrated systems has many advantages, including its powerful ability to simulate complex geometries and distributed physical properties, as well as its high flexibility in simulating complex material behavior and nonlinear problems. At the same time, it can provide detailed numerical solutions of local stress and deformation. However, FEM also has some shortcomings, such as the large amount of computing resources and time required to create the model, and the numerical instability that may occur when the model becomes too complex. HAN et al. [33] solved Maxwell's equations in integral form and proposed an effective method for TSV modeling using integral equations combined with global modal basis functions.

FVM divides the solution domain into multiple independent small volume units and connects them together through grid points. XIE et al. [34] proposed FVM based on non-uniform grid for DC voltage drop simulation of three-dimensional power transmission network (PDN). This method considers the correlation between resistivity and position in the finite volume formula, thereby enabling the simulation of power transmission networks with non-uniform resistivity.

II. THERMAL SIMULATION DESIGN ANALYSIS

Although the use of multi-chip stacking technology is beneficial to the development of miniaturized integrated circuits, it also significantly increases power density and reduces cooling efficiency, which makes three-dimensional integrated systems face more severe thermal challenges. The lengthening of the pathway from each chip to the heat sink, alongside the heightened thermal resistance and the formation of localized hot spots, results in a persistent increase in system temperature, which adversely impacts the performance, dependability, and longevity of the integrated system. Consequently, it is essential to perform comprehensive study and analysis of the thermal performance of three-dimensional integrated systems, as well as to forecast and regulate their temperatures. In the thermal simulation design of a three-dimensional integrated system utilizing TSV vertical interconnection, it is imperative to thoroughly consider several critical design parameters, including the TSV structure, material properties, power consumption distribution across layers, operating frequencies of devices and circuits, and thermal resistance between chips, among others. Currently, analytical and numerical models are predominantly employed to investigate issues in the field.

2.1 Thermal simulation design based on analytical model

LAN [35] and others use simple concepts and theoretical resistance network models and redesign PCB parameters or materials to improve thermal failures. The comprehensive thermal analysis process established is shown in Figure 6. Despite its computational efficiency and modeling simplicity, this method's suitability is restricted to solving steady-state thermal problems with simple 3D geometries, where high accuracy is not critical. The analytical heat algorithm was advanced by HUANG et al [36, 37] through the application of generalized integral transformation. Its calculation speed is improved compared with the algorithm based on Green's function derivation, and the maximum error is 0.3576%. The improved analytic heat algorithm flow is shown in Figure 7 Show. In addition, LIU et al. [38] introduced a novel TSV

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thermal resistance model accounting for copper and oxide layer effects, significantly improving FDM thermal simulation accuracy when integrated with their lateral thermal model. ZHAN et al. [39] developed an analytical thermal algorithm for integrated circuits using Green's function, enabling the calculation of steady-state temperatures across the entire chip with adjustable accuracy. JAIN et al. [40] introduced a simplified thermal modeling approach, reducing 3D integrated systems to 1D thermal resistance models, allowing for efficient thermal analysis with some loss of precision in inter-layer temperature measurements.

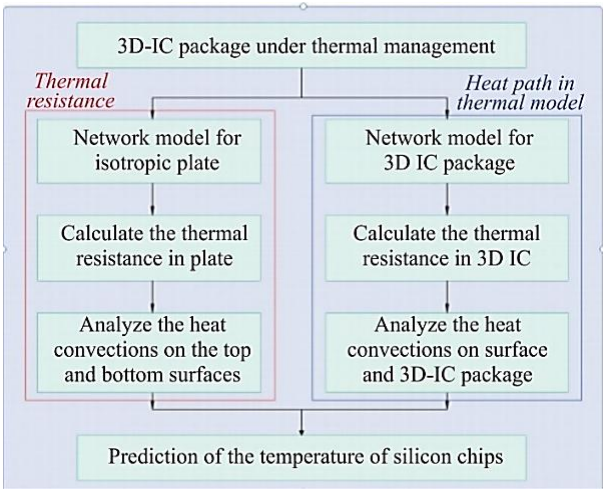

Figure 6: Comprehensive analysis process

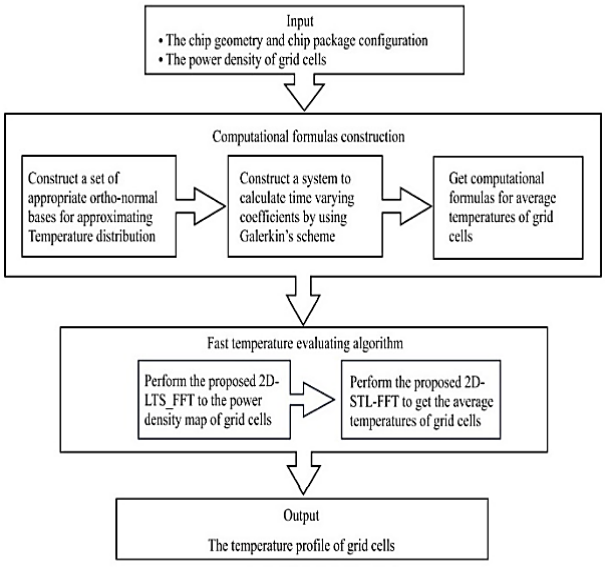

Figure 7: improved analytical algorithm

2.2 Thermal simulation design based on numerical calculation model

In contrast to analytical models, numerical calculation models offer enhanced practicability and accuracy in solving thermal problems within 3D integrated systems, although they are susceptible to error accumulation and high computational costs. WANG et al. [41] assessed the transient thermal behavior of a 3D chip using an alternating implicit approach, leveraging unconditional steady-state characteristics and finite element analysis, a method renowned for its high simulation accuracy in 3D integrated systems. Studies by Kuo et al. [42] focused on thermal aspects of system-level packaging TSV using FDM. FU et al. [43] subsequently proposed a triangular TSV cluster layout, improving heat dissipation efficiency without area increase. Simulation outcomes showed notable temperature decreases: 0.22% average, 1.69% peak (vertical), and 0.10% (lateral). Research by ZHU et al. [44] involved solving the heat conduction equation via FDM, followed by the application of advanced numerical techniques, including Minimum Residual Method and SSOR preconditioning, to accurately determine the temperature matrix. TODRI [45] proposed a 10-layer system leveraging existing 3D technical specifications, enhancing power delivery by modifying TSV physical design and reducing peak temperatures. However, this approach has limited effectiveness in improving heat dissipation efficiency in 3D integrated systems through optimized TSV physical properties and arrangement. HOE et al. [46] investigated the impact of TSV physical dimensions on thermal conductivity and found that optimization can improve 3D integrated system thermal performance. Figure 8 presents TSV geometries with varying aspect ratios, highlighting the effect of dimension adjustments while maintaining a fixed through-hole size.

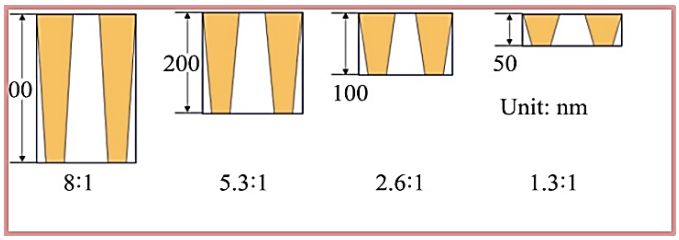

Figure 8: TSV geometries with different aspect ratios (via size fixed)

III. ELECTROTHERMAL COUPLING SIMULATION DESIGN AND PROBLEM ANALYSIS

As the integration level of integrated circuits increases, the problem of Joule heat generated during signal coupling and signal propagation becomes increasingly serious. Under the influence of external electrostatic discharge (ESD), the reliability of circuits is severely challenged. Conduction losses caused during signal transmission are converted into heat. When this heat cannot be dissipated effectively, the temperature of the circuit will rise rapidly. Such temperature rise not only changes the electrical properties of the material and increases conduction losses, but may also cause the material to undergo thermal stress exceeding its limit and suffer damage. During the design process of three-dimensional

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integrated circuits, a cross-domain collaborative design must be adopted to ensure systematic integration of electrical.

3.1 Mechanism and impact of electrothermal coupling

In 3D-IC, TSV not only assumes the responsibility of transmitting electrical signals due to its role of vertical interconnection, but also becomes the main channel for heat transfer. TSV contains metallic materials (such as copper, etc.), which itself generates Joule heat when current passes through it. Due to the dense layout of TSVs, especially when the TSVs are at the center or bottom of the chip, this heat may not be effectively transferred to the chip surface for heat dissipation. As the power density inside 3D-IC increases, TSV becomes a hot spot for heat accumulation. The formation of hot spots is closely related to the material properties of TSV, the size and distribution of current, and the heat transfer capability in the surrounding environment. The nonlinear coupling between thermal field and electric field mainly includes two situations. The electric field generates Joule heat. As a heat source of the thermal field, the distribution of the thermal field can be obtained, that is, coupling is performed by providing a field source. To determine the thermal field distribution, we follow a sequential approach: first, the current continuity equation is solved to obtain the potential distribution; next, the thermal field source is derived from the potential distribution; finally, the heat conduction equation is solved to yield the thermal field distribution. The temperature field realizes the coupling of the two physical fields by affecting the material parameters of the model (such as electrical conductivity, thermal conductivity, thermal expansion coefficient, etc.). part Material parameters do not change with temperature changes, that is, non-temperature changing material parameters, such as material density, Poisson's ratio and heat capacity, can be regarded as constants when the temperature changes, and generally take their values at room temperature.

3.2 Electric and thermal coupling simulation design

WANG et al. [47] investigated the impact of temperature on TSV parasitic resistance and capacitance by integrating copper properties with an equivalent circuit model. Building on this work, ZHAO et al. [48] extended coaxial TSV theory and performed an in-depth analysis of parasitic effects. Furthermore, KATTI et al. [49] experimentally confirmed the temperature-dependent effects on TSV parasitic parameters. Meanwhile, WANG et al. [50] employed finite element analysis to investigate heat distribution and electric field distribution, and explored the electrothermal characteristics by adjusting the voltage amplitude and TSV oxide layer thickness. LU et al. [51-53] conducted a comprehensive study on electrothermal coupling in TSV arrays and power transmission using finite element analysis. The investigation covered steady-state temperature distribution, DC voltage drop, and high-frequency S-parameters to characterize network behavior. SAI et al. [54] developed a nonlinear electrothermal delay model to investigate three-dimensional integrated systems based on Through-Silicon Vias (TSVs), introducing the concept of "virtual TSV". Balancing temperature and stress gradients, the research results show that according to the proposed model, clock offset can be reduced by 61.3% on average. Based on the thermoelectric analogy principle, JIANG et al. [55] utilized electrical simulation software to perform steady-state thermal analysis of large-scale interconnect structures. Lowering chip temperature and reducing hot spots are very effective in preventing material performance changes caused by temperature changes. By changing parameters such as radius, spacing, insulation layer thickness, and using new materials such as CNT, the heat dissipation performance of TSV can be improved, thereby reducing the impact of electrothermal coupling. CHEN et al. [56] proposed a thermally aware via layout technology to minimize lateral thermal blocking caused by dense signal bus TSV structures. SAHA et al. [57] proposed a method based on guided genetic algorithm (GA) to solve the placement and allocation problem of TSV. GRZESIAK-KOPEC et al. [58] proposed a knowledge-intensive 3D-IC layout diagram representation method and elaborated on the neighborhood optimization heuristic method, whose goal is to minimize the total length of interconnection lines between subcircuits. SATOMI et al. [59] introduced an optimization technique for thermal component placement on PCBs, employing genetic algorithms to reduce maximum temperature and inter-component wire length. SRIKANTH et al. [60] proposed a multi-objective geometric optimization method for matrix composite radiators based on phase change materials (PCM) to improve the energy efficiency and performance of the radiator.

3.3 Analysis and summary of solutions to electrothermal coupling problems

As the density of integrated circuits increases, the electrothermal coupling problem has become one of the key factors affecting the reliability and performance of 3D integrated circuits. The effectiveness of thermal management strategies for 3D integrated circuits is directly related to the effectiveness of overall design and layout optimization. Through the application of diverse electrothermal simulation design and analysis techniques, researchers have developed solutions to enhance TSV thermal performance, mitigate hotspots, reduce thermal stress, and ultimately boost chip reliability and performance. A crucial aspect of understanding electrothermal coupling mechanisms and impacts involves elucidating Joule heat generation and temperature's influence

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on circuit electrical characteristics. The simulation design methods proposed by researchers from all parties, such as thermoelectric distribution simulation based on finite element analysis and research on the impact of temperature on TSV resistance and capacitance, all provide powerful tools for understanding and dealing with electrothermal coupling problems. In terms of solutions, researchers have explored different approaches, including improving the material and structural design of TSVs, optimizing TSV layout, and adopting advanced heat dissipation technology. Through simulation and numerical analysis, they have proposed algorithms including CNT and minimum cost flow layer distribution, genetic algorithms, etc. to improve the thermal management of the chip. These methods not only help improve thermal conductivity, but also have a positive effect on improving the overall electrical characteristics of the circuit. To sum up, in order to ensure the successful implementation of high-density integrated circuit design, the electrothermal coupling issue must be highly concerned and systematically considered, and the proposal of simulation design methods and solutions is the cornerstone to ensure the feasibility of 3D-IC technology. In the future, with the continuous exploration of new materials, new design methods and the continuous deepening of the understanding of electrothermal coupling effects, there is reason to believe that integrated circuit design will be able to deal with electrothermal coupling issues more effectively, paving the way for the development of high-performance electronic devices.

IV. CONCLUSION

In modern microelectronics technology, with the increase of integration level and power consumption, the electrothermal coupling problem has become one of the factors limiting the further improvement of 3D-IC performance. Excessive heat accumulation may cause local temperature increases, affecting material properties and system reliability. This article reviews the research progress of electrothermal coupling simulation design of three-dimensional integrated systems based on TSV, provides a basis for in-depth analysis and understanding of electrothermal coupling issues, and discusses possible solution strategies to ensure the reliability and performance of 3D-IC guide. As 3D integration continues to advance, 3D-ICs face a critical challenge: mitigating electrical and thermal coupling effects that worsen with increased power consumption. In the future, it is necessary to further research and develop new design methods and materials, and at the same time further improve the accuracy and efficiency of simulation design, which can help designers better Predict and solve electrothermal coupling problems. In addition, attention needs to be paid to the reliability of 3D-ICs and the optimization of manufacturing processes to promote their widespread application. In summary, 3D-1C faces many challenges, but it also has broad development prospects and requires interdisciplinary cooperation and sustained research efforts.

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